ABSTRACT OF THE DISCLOSURE

METHOD AND SYSTEM FOR DEFECT EVALUATION USING QUIESCENT POWER PLANE CURRENT (IDDQ) VOLTAGE LINEARITY

A method and system for defect evaluation using IDDQ voltage linearity provides improved IDDQ testing for determining whether manufacturing defects in a VLSI device are likely to cause functional faults. IDDQ data is collected at multiple power plane voltages (VDDs) for a test vector at which a fault is activated. The IDDQ vs. VDD is then examined and a range of VDDs over which the characteristic IDDQs are non-linear with respect to VDD is determined. Peaks in the first derivative of the IDDQ vs. VDD curve indicate a particular VDD at which the onset of non-linearity in the IDDQ occurs. The VDD point below which the curve is non-linear indicates the relative resistance of a fault with respect to the driving point resistance of the node at which the fault is located. The relative resistance is directly determinative of additional circuit delay cause by the fault and/or whether the fault will cause a logic level transmission failure. Therefore, the range of VDDs for which the IDDQ curve is linear provides a pass/fail indication that can be used to reject devices in manufacturing test.